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Signature: Shirley Fajardo

PATENT
Docket No. P1025

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: ROBERT B. OGLE, JR.
MARK T. RAMSBEY
TUAN DUC PHAM

SERIAL NO.: 09/607,675

FILED: JUNE 30, 2000

FOR: DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER
FOR FLASH MEMORY AND OTHER DUAL GATE
TECHNOLOGIES AND METHOD OF FORMING

Assistant Commissioner of Patents
Office of Initial Patent Examination
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Washington, D.C. 20231

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TRANSMITTAL LETTER

Dear Sir:

In connection with the above-referenced patent application, transmitted herewith are the following:

1. Request For Corrected Filing Receipt (2 pages);
2. Copy of Original Filing Receipt with corrections made on the document in red ink (2 pages);

D931

3. Copy of first page of Patent Application (1 page); and
4. Post card in acknowledgment of all transmitted materials.

Please date-stamp the enclosed post card and return same to the undersigned in acknowledgment of receipt of all transmitted materials.

Respectfully submitted,



Victor Flores

Reg. No. 29,638

VF/sf

October 17, 2000

LARIVIERE, GRUBMAN & PAYNE, LLP

P.O. Box 3140

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(831) 649-8800

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Washington, D.C. 20231

REQUEST FOR CORRECTED FILING RECEIPT

Dear Sir:

Attached is a copy of the Original Filing Receipt received in connection with the above-referenced patent application, for which issuance of a corrected filing receipt is respectfully requested.

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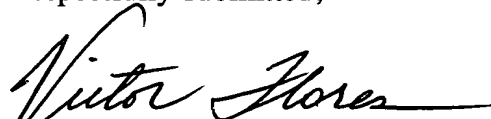
1. There is an error in the:

 X Continuing Data as Claimed by Applicant, in that it should read as follows:

THIS APPLICATION CLAIMS PRIORITY BENEFIT TO U.S. PROVISIONAL
APPLICATION 60/159,235 FILED 10/13/99; AND

Please delete the 06/13/1980 Pat 4,308,791 this information does not refer to this
application.

Respectfully submitted,



Victor Flores
Reg. No. 29,638

VF/sf

October 17, 2000

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/607,675	06/30/2000	2811	768	P1025	6	13	4

LARiviere Grubman & Payne LLP
P O Box 3140
Monterey, CA 93942-3140

Date Mailed: 08/25/2000

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the PTO processes the reply to the Notice, the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)Robert B. Ogle JR., San Jose, CA ;
Tuan D. Pham, San Jose, CA ;
Mark T. Ramsbey, Sunnyvale, CA ;**Continuing Data as Claimed by Applicant**

THIS APPLN CLAIMS BENEFIT OF 06/159,235/06/13/1980 PAT 4,308,791

This Application claims priority benefit to U.S. Provisional Application
Foreign Applications

60/159,235 filed 10/13/99.

If Required, Foreign Filing License Granted 08/21/2000

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TitleDual-purpose anti-reflective coating and spacer for flash memory and other dual gate technologies
and method of forming**Preliminary Class**

252

Data entry by : LEGESSE, ALTAYEWORK

Team : OIPE

Date: 08/25/2000



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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**



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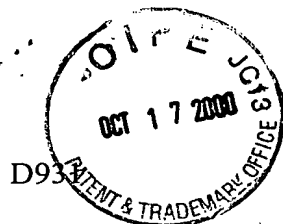
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PATENT
Docket No. P1025

PATENT APPLICATION

DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH
MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD OF FORMING

INVENTORS: ROBERT B. OGLE, JR.
MARK T. RAMSBEY
TUAN DUC PHAM

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RELATED APPLICATION

TECHNOLOGY CENTER 2800

This application is related to co-pending U.S. Provisional Patent Application Ser. No. 60/159,235, entitled "DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD OF FORMING", filed October 13, 1999.

TECHNICAL FIELD

The present invention relates to integrated semiconductor circuits and anti-reflective coating fabrication techniques used in dual gate semiconductor technology, such as FLASH memory technology. More particularly, the present invention relates to integrated semiconductor circuits and fabrication techniques for forming sidewall structure on the sidewalls of the transistor gates used in dual gate semiconductor technology, such as FLASH memory technology. Even more particularly, the present invention relates to integrated semiconductor circuits and fabrication techniques for forming sidewall structure on the sidewalls of transistor gates in the core memory region as used in dual gate semiconductor technology, such as FLASH memory technology.